



V_{DS} 30 V
 I_D 60 A
 $R_{DS(ON)}$ (at $V_{GS}=10V$) 3.2 mohm
 $R_{DS(ON)}$ (at $V_{GS}=4.5V$) 4.0 mohm
 100% UIS Tested
 100% VDS Tested

Trench Power LV MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$

DC-DC Converters
 Power management functions
 Backlighting

($T_A=25$ unless otherwise noted)

Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25$	I_D	60	A
	$T_C=100$		38	
Pulsed Drain Current ^A		I_{DM}	240	A
Total Power Dissipation @ $T_C=25$ ^B		P_D	75	W
Total Power Dissipation @ $T_C=100$ ^B		P_D	30	W
Total Power Dissipation @ $T_A=25$ ^C		P_D	6.2	W
Single Pulse Avalanche Energy ^D		E_{AS}	400	mJ
Thermal Resistance Junction-to-Case		R_{JC}	1.67	/W
Thermal Resistance Junction-to-Ambient		R_{JA}	20	/W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

(Example)

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(T_J=25 unless otherwise noted)

Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =20A		2.6	3.2	m
		V _{GS} = 4.5V, I _D =20A		3.4	4.0	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.85	1.2	V
Gate resistance	R _g	F=1 MHz, Open drain		2.9		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		4498		pF
Output Capacitance	C _{oss}			800		
Reverse Transfer Capacitance	C _{rss}			643		
Total Gate Charge	Q _g (10V)	V _{GS} =10V, V _{DS} =15V, I _D =20A		92.7		nC
Total Gate Charge	Q _g (4.5V)			46		
Gate-Source Charge	Q _{gs}			13.5		
Gate-Drain Charge	Q _{gd}			22.8		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=500A/us		3.0		
Reverse Recovery Time	t _{rr}			15		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =4A, R _L =0.75 R _{GEN} =3		11		ns
Turn-on Rise Time	t _r			80		
Turn-off Delay Time	t _{D(off)}			39		
Turn-off fall Time	t _f			92		

A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. The power dissipation P_D is based on T_{J(MAX)}=150, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. The value of R_{JA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25.

D. T_J=25, V_{DD}=20V, V_G=10V, L=2.0mH, I_{AS}=20A.

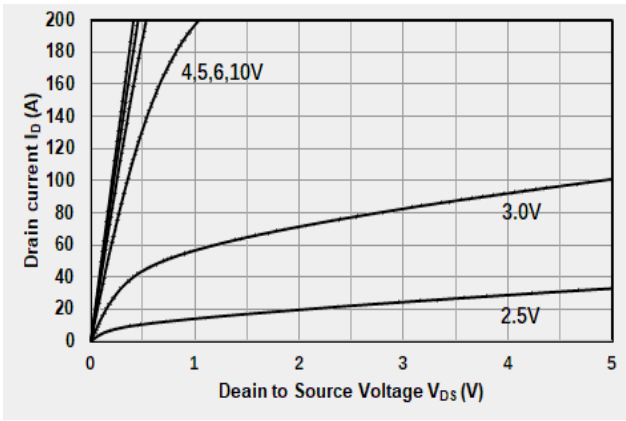


Figure1. Output Characteristics

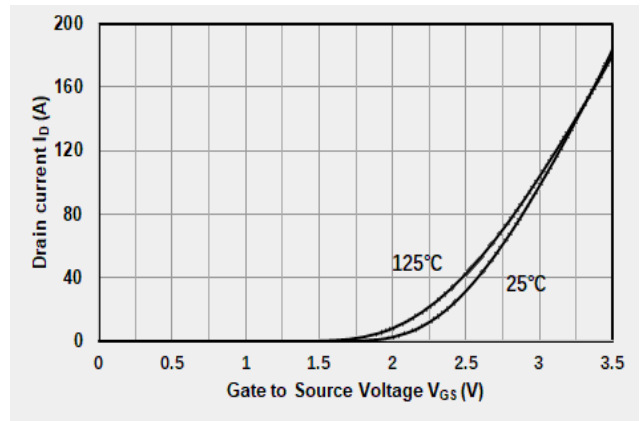


Figure2. Transfer Characteristics

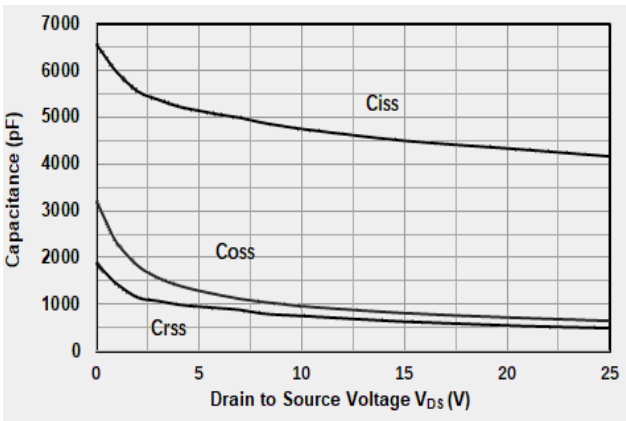


Figure3. Capacitance Characteristics

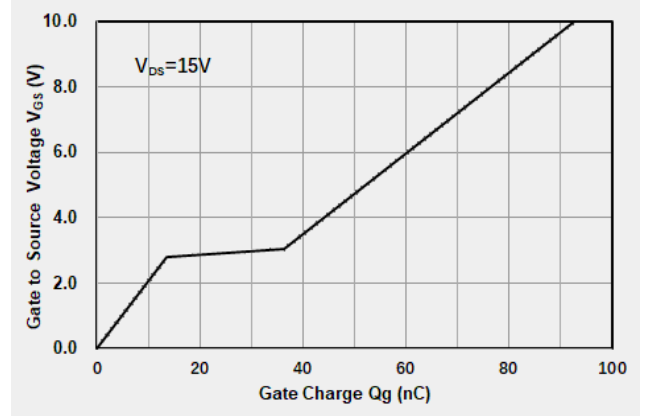


Figure4. Gate Charge

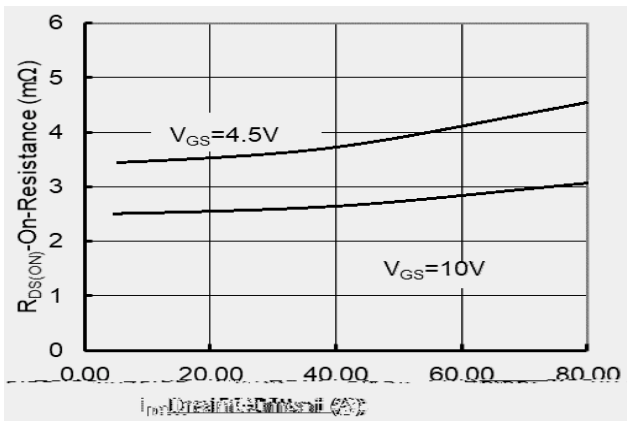


Figure5. Drain-Source on Resistance

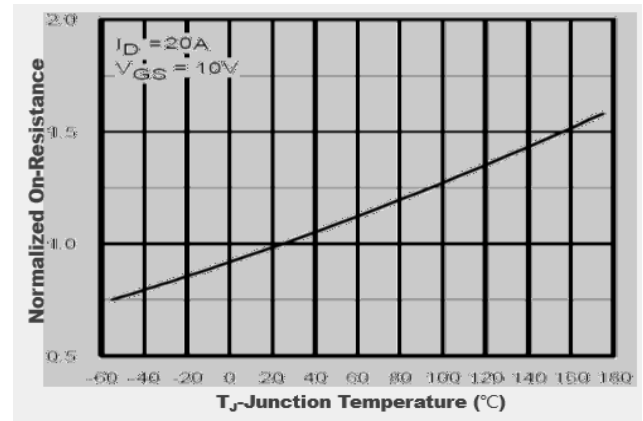


Figure6. Drain-Source on Resistance

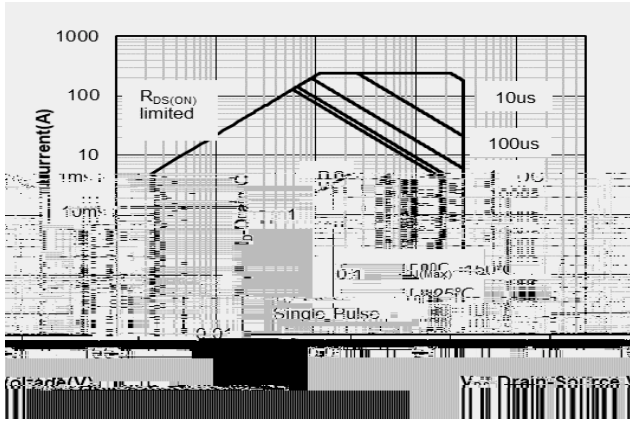


Figure7. Safe Operation Area

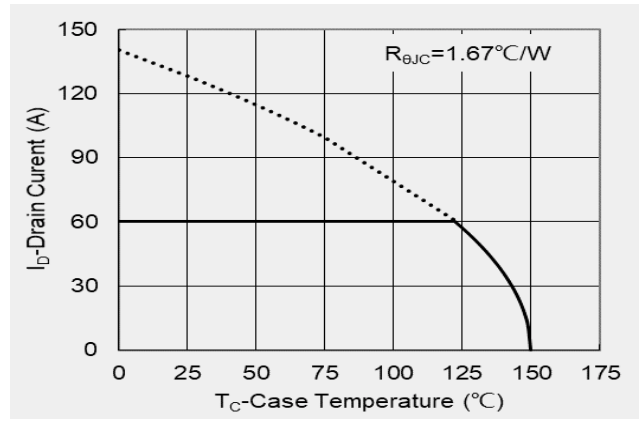


Figure8. Drain current vs. Case Temperature

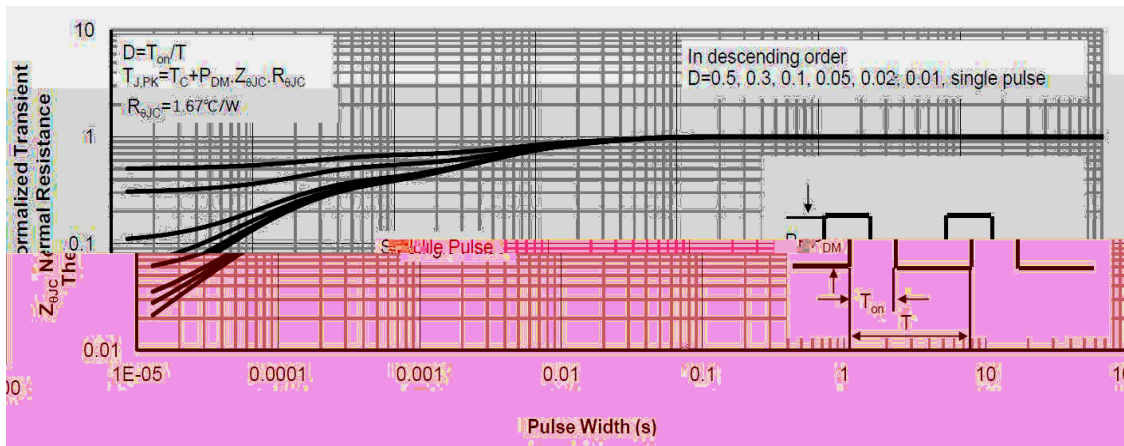


Figure9. Normalized Maximum Transient Thermal Impedance



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