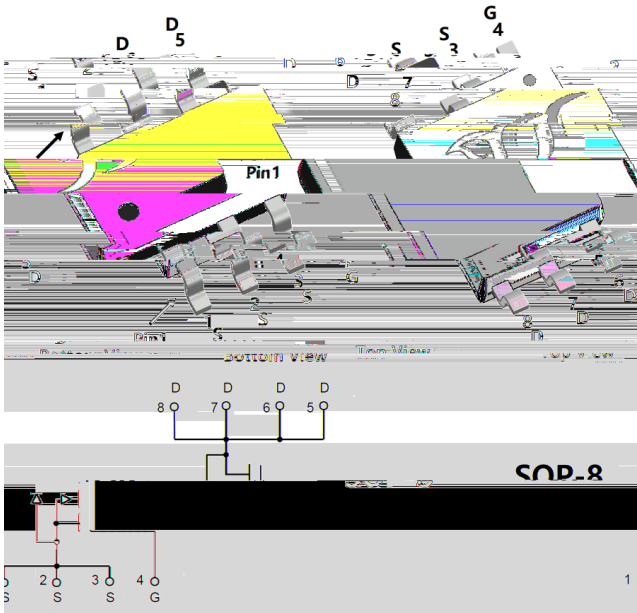




# YJS12G06D

## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

$V_{DS}$	60V
$I_D$	12A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	< 8.5 mohm
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	< 12 mohm
100% EAS Tested	

### General Description

Split Gate Trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 3  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

DC-DC Converters  
 Power management functions  
 Industrial and Motor Drive application

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current (Silicon limited)	$T_A=25^\circ C$	$I_D$	12	A
	$T_A=100^\circ C$		7.5	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	48	A
Avalanche energy <sup>B</sup>		EAS	132	mJ
Total Power Dissipation <sup>C</sup>		$P_D$	3.1	W
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	R	31	40	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		59	75	
Thermal Resistance Junction-to-Case	Steady-State	$R_L$	16	24	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS12G06D	F2	Q12G06D	4000	8000	64000	13 reel



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## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		1	
			T <sub>J</sub> =55°C		5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R <sub>Ds(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =12A		6.8	8.5	m
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A		8.3	12	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =12A, V <sub>GS</sub> =0V		0.85	1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				12	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =35V, V <sub>GS</sub> =0V, f=1MHZ		2000		pF
Output Capacitance	C <sub>oss</sub>			390		
Reverse Transfer Capacitance	C <sub>rss</sub>			13		
Gate Resistance	R <sub>g</sub>	f=1MHZ, Open drain		1.6		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub> (10V)	V <sub>DS</sub> =30V, I <sub>D</sub> =12A		34		nC
Total Gate Charge	Q <sub>g</sub> (4.5V)			15.8		
Gate-Source Charge	Q <sub>gs</sub>			7.8		
Gate-Drain Charge	Q <sub>gd</sub>			5.2		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =12A, di/dt=200A/us		36		ns
Reverse Recovery Time	t <sub>rr</sub>			27		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =12A R <sub>GEN</sub> =3		10		ns
Turn-on Rise Time	t <sub>r</sub>			36		
Turn-off Delay Time	t <sub>D(off)</sub>			30		
Turn-off fall Time	t <sub>f</sub>			57		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub> 0.5mH, I<sub>AS</sub>=23A,.

C. Pd is based on max. junction temperature, using ≤10s junction-ambient thermal resistance.

D. The value of R is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on R junction temperature of 150° C. The value in any given application depends on the user's specific board design.



## Typical Performance Characteristics

Figure1. Output Characteristics



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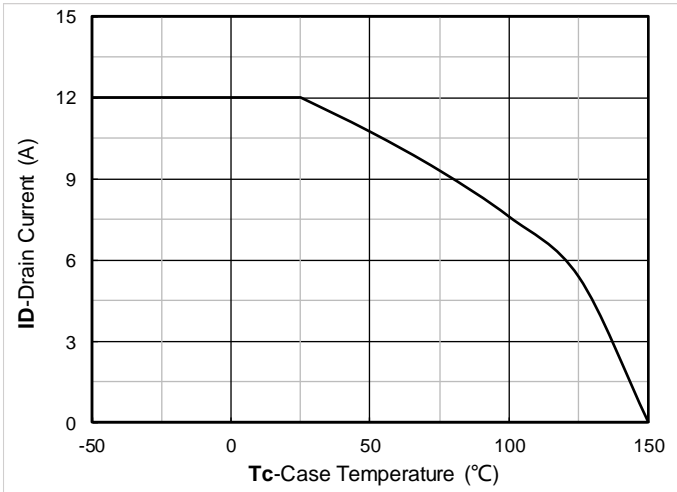


Figure7. Drain current

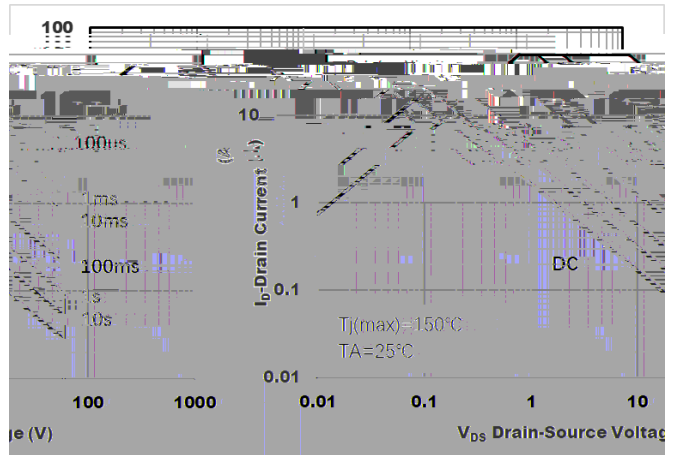


Figure8. Safe Operation Area

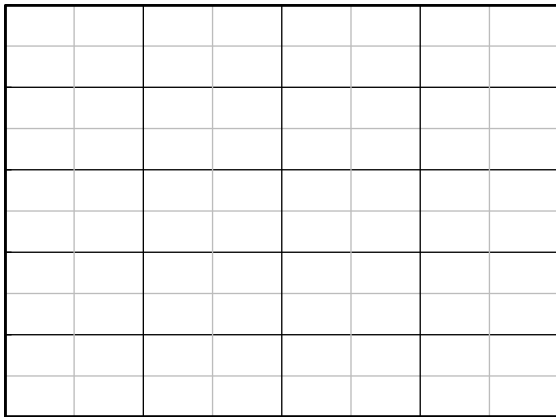


Figure 9. On-Resistance vs Gate to Source Voltage

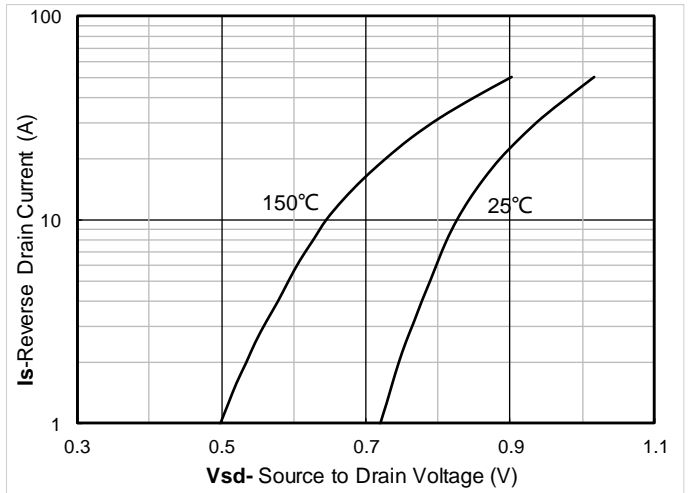


Figure 10. Forward characteristics of reverse diode

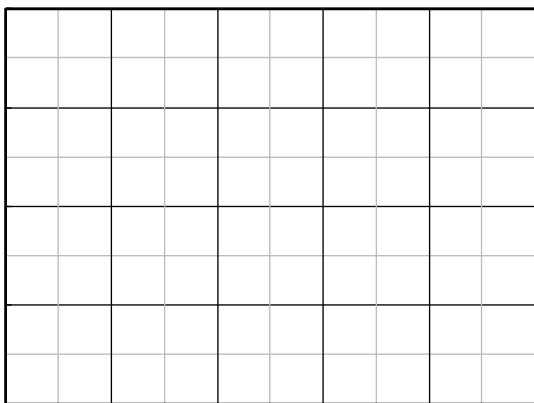


Figure 11. Normalized breakdown voltage

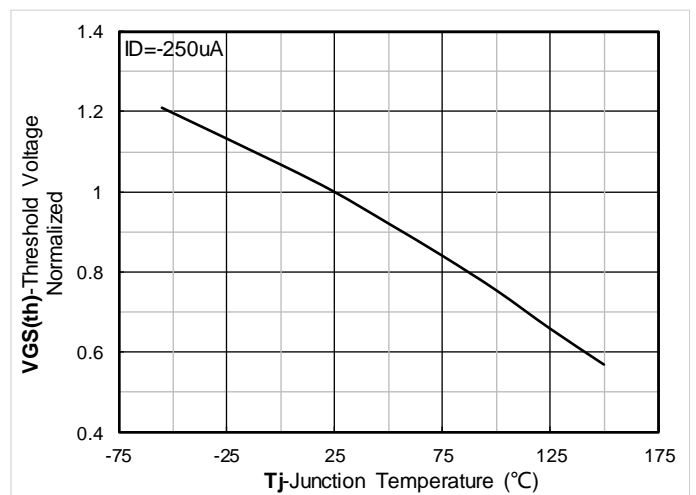


Figure 12. Normalized Threshold voltage



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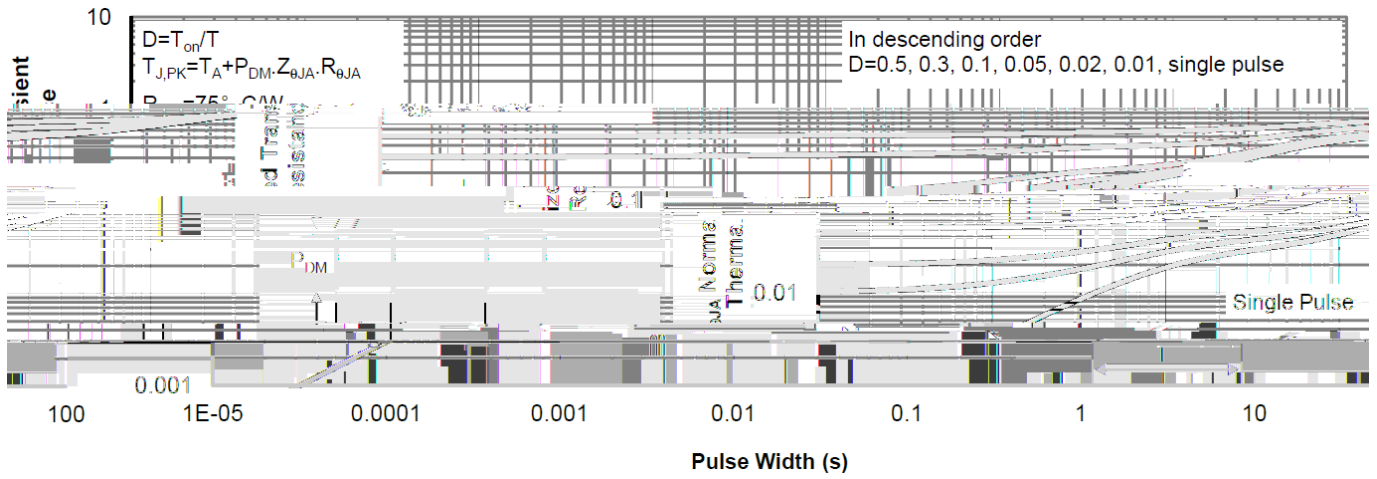
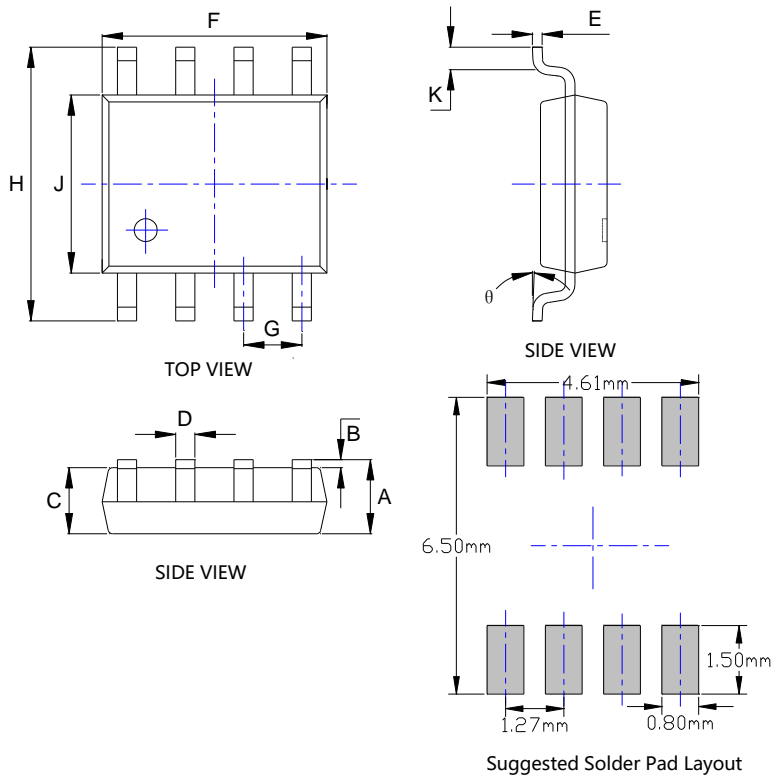


Figure13. Normalized Maximum Transient Thermal Impedance



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## SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
$\theta$	0°	8°	0°	8°

**Note:**  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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