



YJS15G10A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	15A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	9.5 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	12.5 mohm
100% EAS Tested	

General Description

Split Gate Trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$

Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

DC/DC Primary Side Switch
Telecom/Server
Synchronous Rectification

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	15	A
	$T_A=100$		9.5	
Pulsed Drain Current ^A		I_{DM}	75	A
Avalanche Energy, Single Pulse(L=0.5mH)		E_{AS}	200	mJ
Total Power Dissipation ^B		P_D	3.8	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

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Typical Performance Characteristics

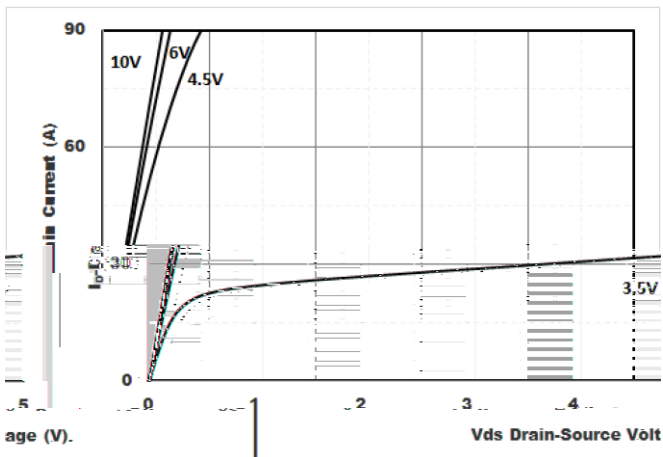


Figure1. Output Characteristics

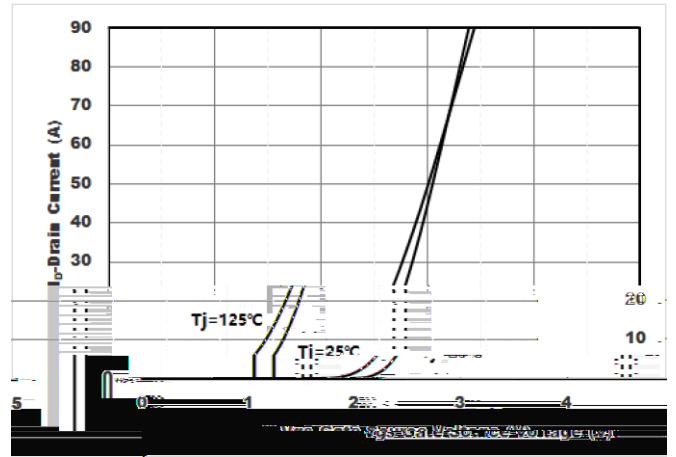


Figure2. Transfer Characteristics

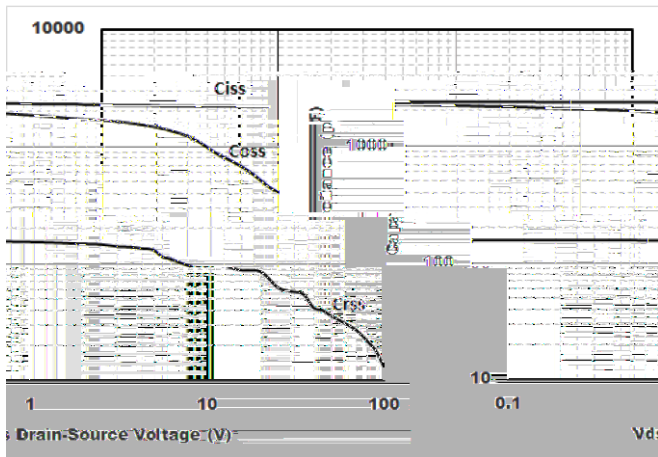


Figure3. Capacitance Characteristics

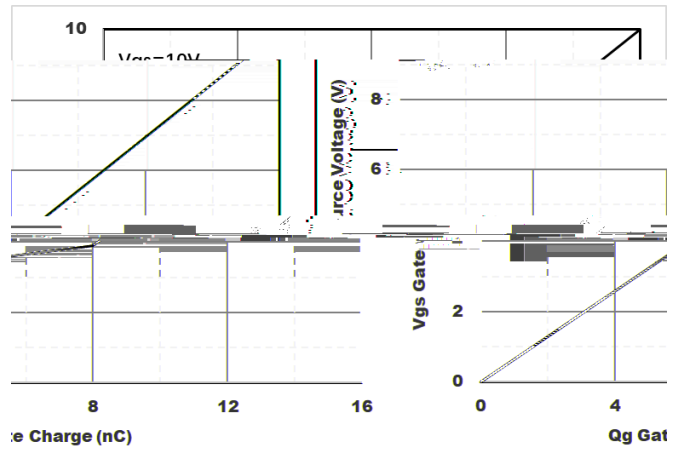


Figure4. Gate Charge

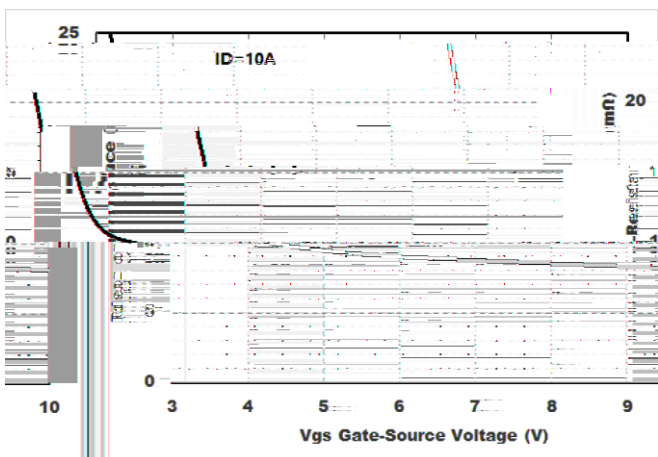


Figure5. Drain-Source on Resistance

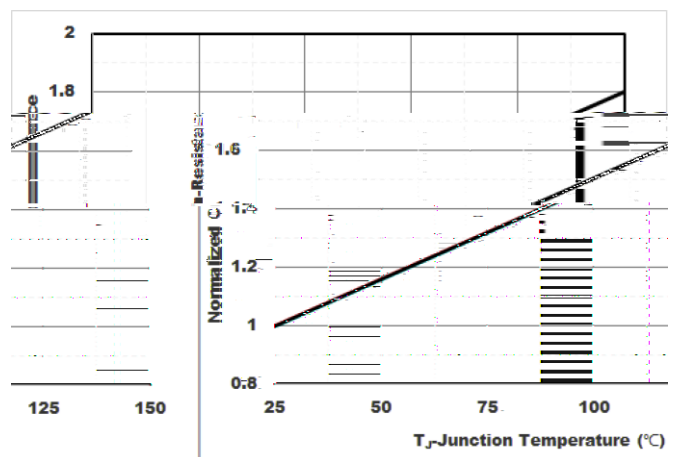


Figure6. Drain Current



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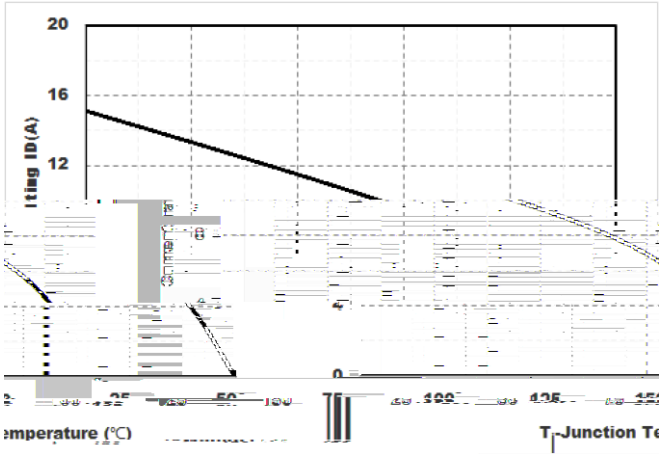


Figure7. Drain current

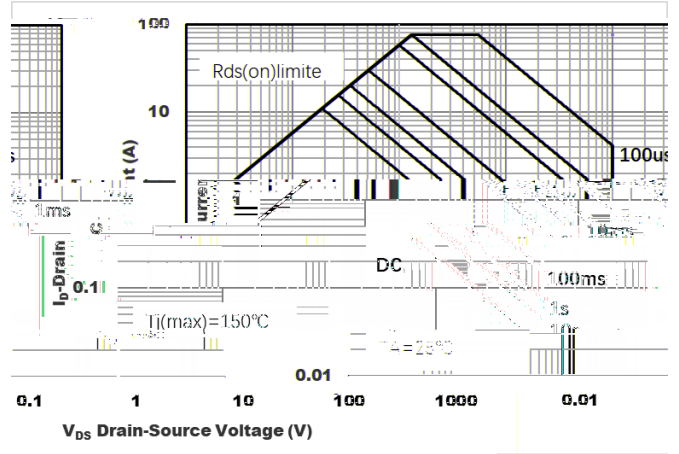


Figure8. Safe Operation Area

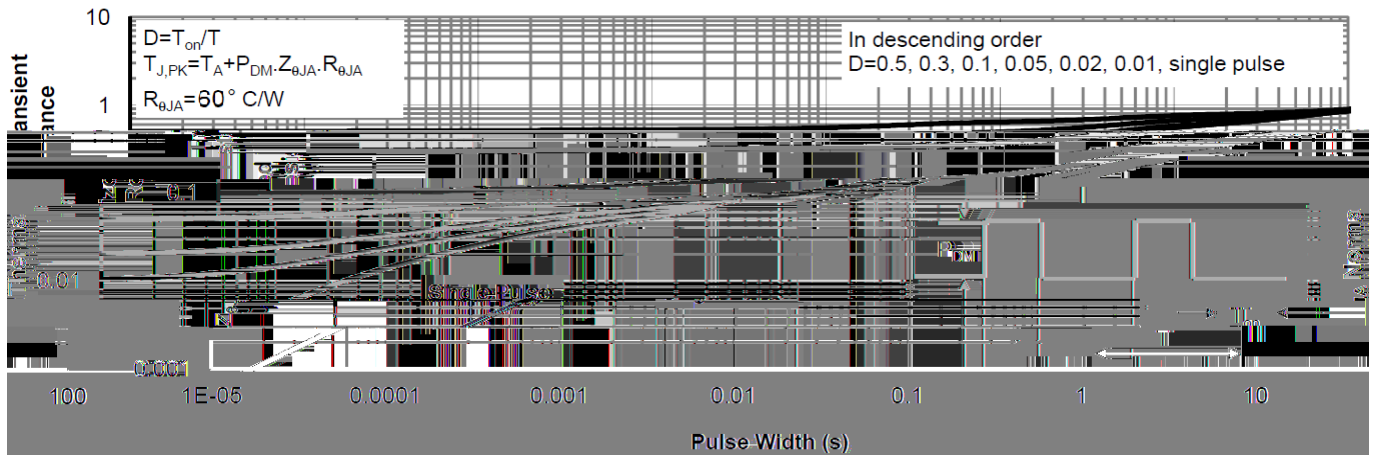
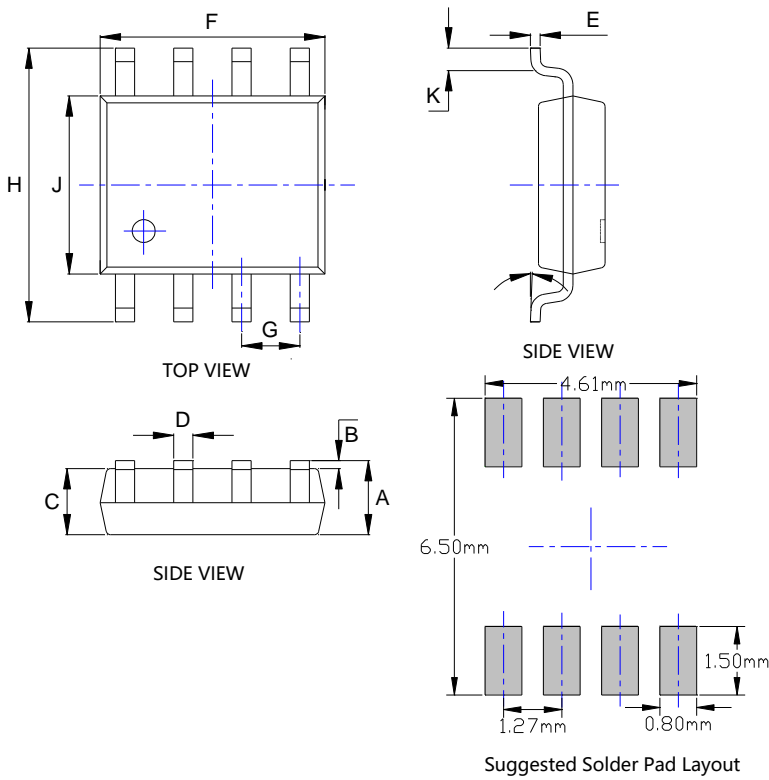


Figure9. Normalized Maximum Transient Thermal Impedance



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SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
	0°	8°	0°	8°

Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.05 mm.
 3. The pad layout is for reference purposes only.

