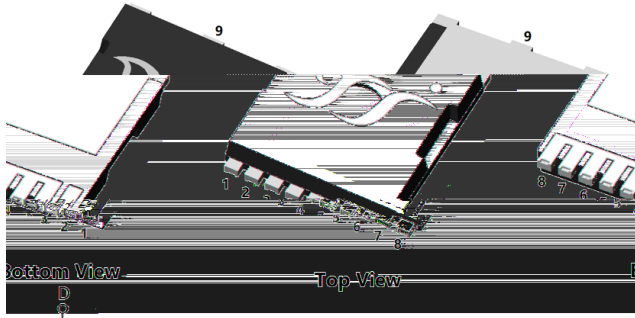




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

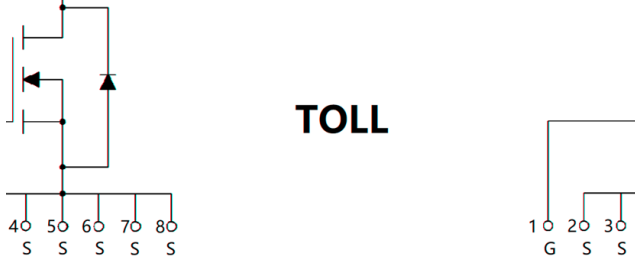
V_{DS}	100V
I_D	280A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	2.3m
$R_{DS(ON)}$ (at $V_{GS}=6V$)	3.5m
100% EAS Tested	
100% V_{DS} Tested	

General Description

- Double trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High Power switching application
- BMS



Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	28	A
	$T_A=100$		17.7	
	$T_C=25$		280	
	$T_C=100$		177	
Pulsed Drain Current ^A		I_{DM}	900	A
Avalanche energy ^B		EAS	2250	mJ
Total Power Dissipation ^C	$T_A=25$	P_D	3.5	W
	$T_A=100$		1.4	
	$T_C=25$		250	
	$T_C=100$		100	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R	30	35	/W
Thermal Resistance Junction-to-Case	Steady-State	R	0.4	0.5	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJT280G10HJ	F1	YJT280G10HJ	2000	4000	20000	13 reel



YJT280G10HJ

RECOMMEND
[YJT300G10H](#)
FOR NEW DESIGN



Typical Electrical and Thermal Characteristics Diagrams

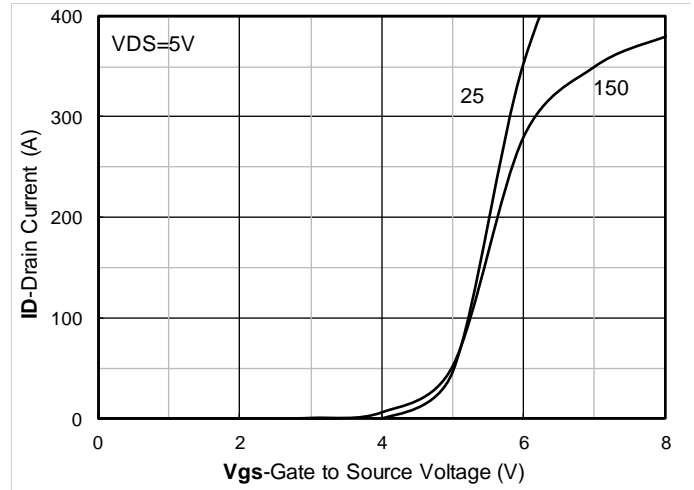


Figure 2. Transfer Characteristics

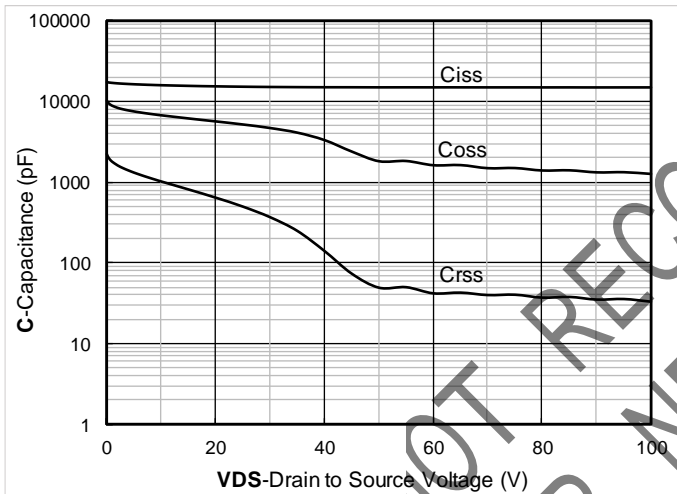


Figure 3. Capacitance Characteristics

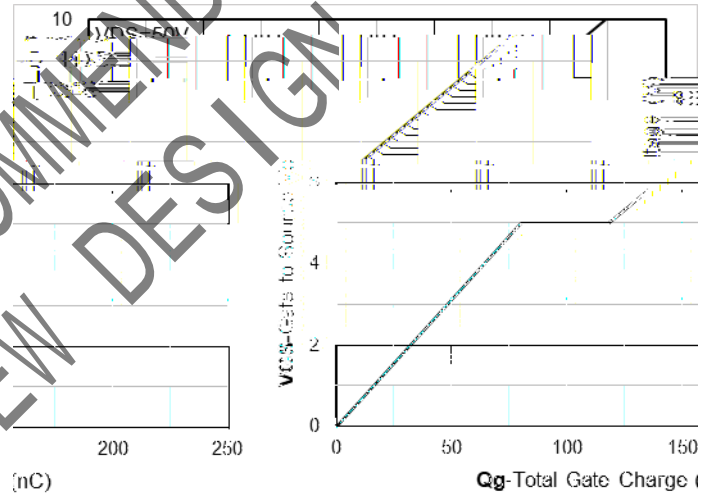


Figure 4. Gate Charge

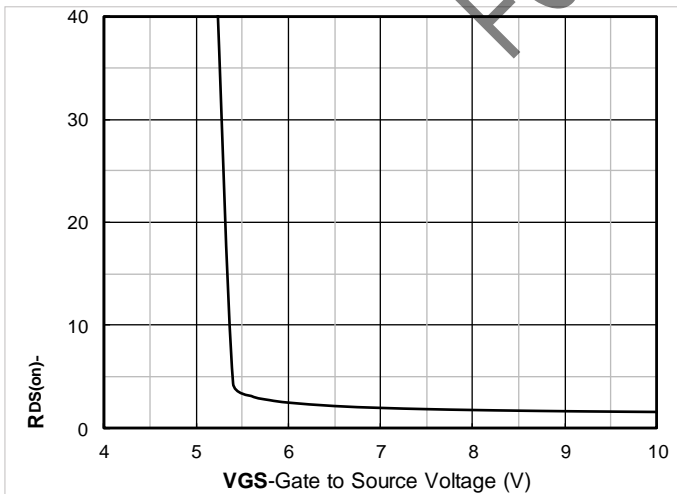


Figure 5. On-Resistance vs Gate to Source Voltage

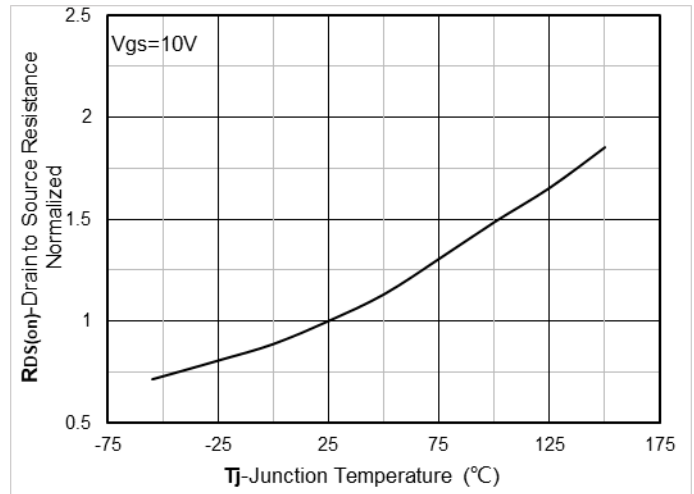


Figure 6. Normalized On-Resistance

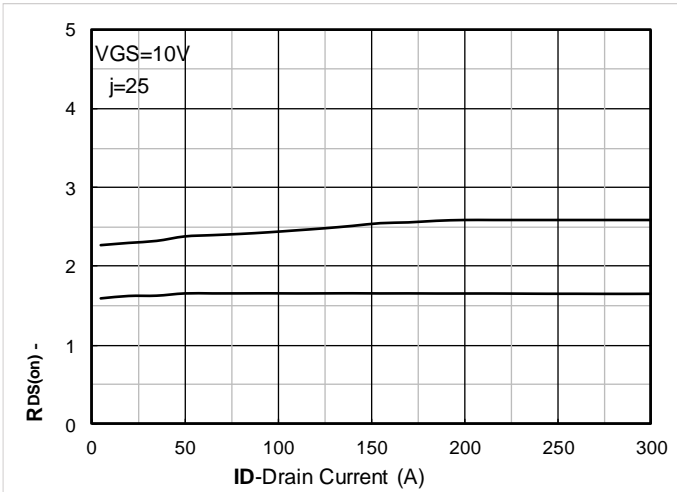


Figure 7. RDS(on) VS Drain Current

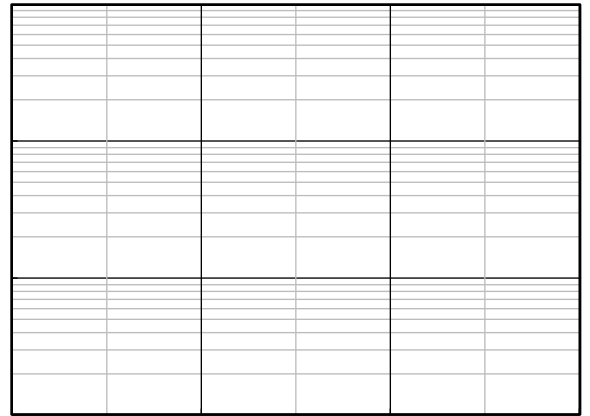


Figure 8. Forward characteristics of reverse diode

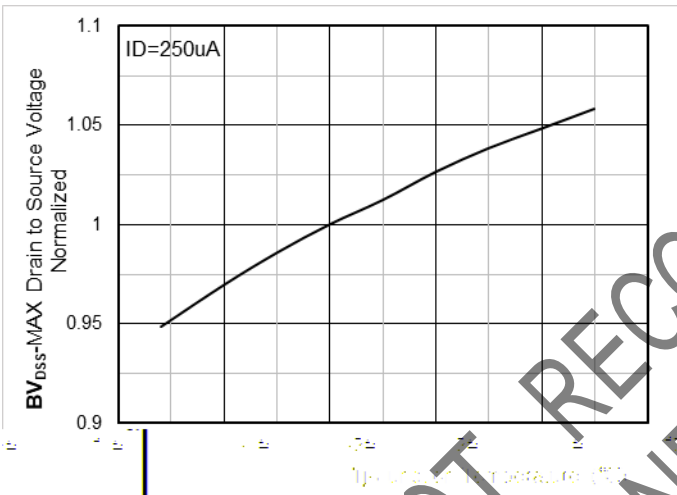


Figure 9. Normalized breakdown voltage

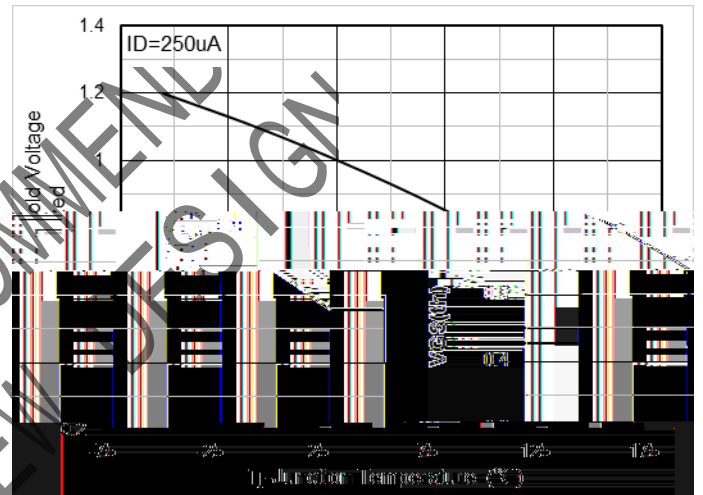


Figure 10. Normalized Threshold voltage

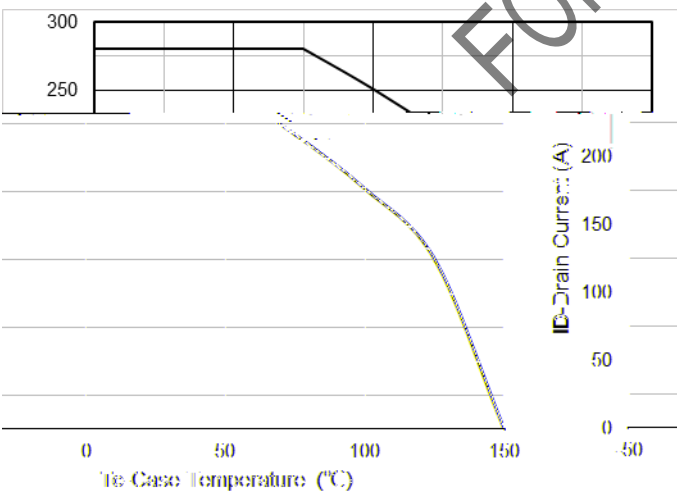


Figure 11. Current dissipation

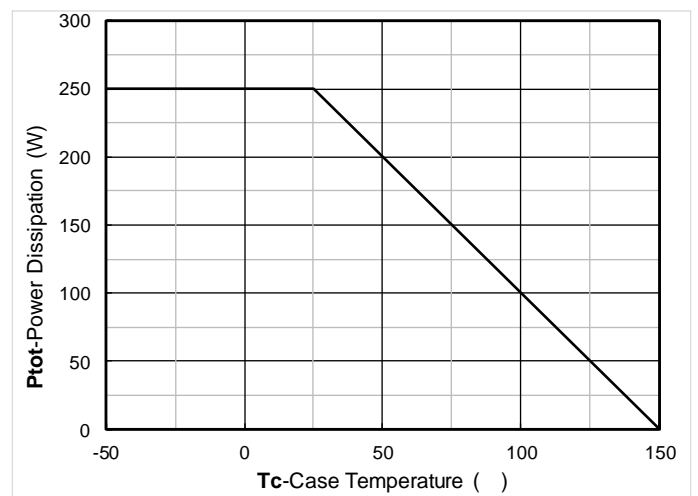
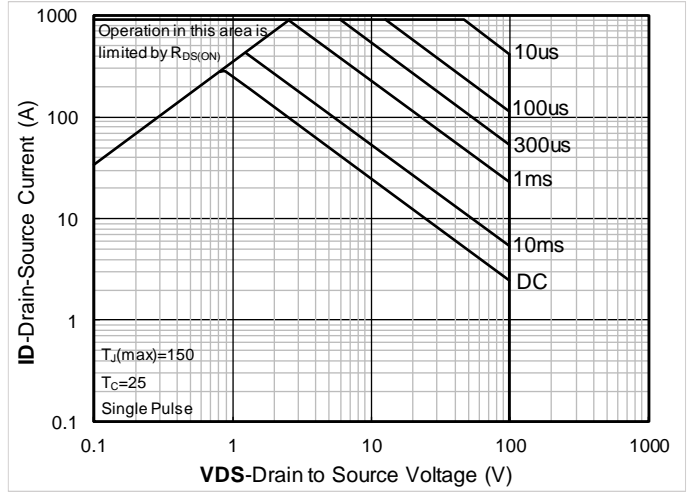
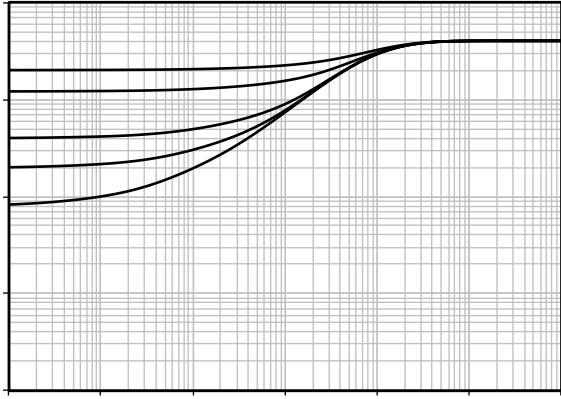


Figure 12. Power dissipation



D.02

Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

Test Circuits & Waveforms

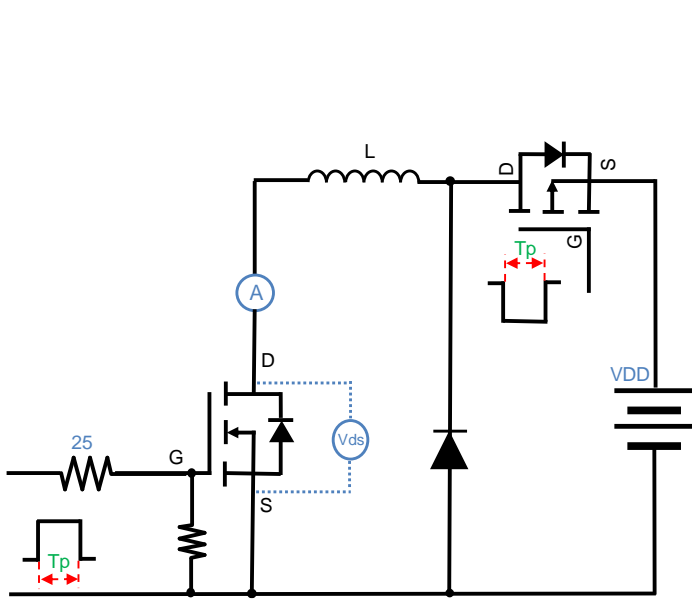
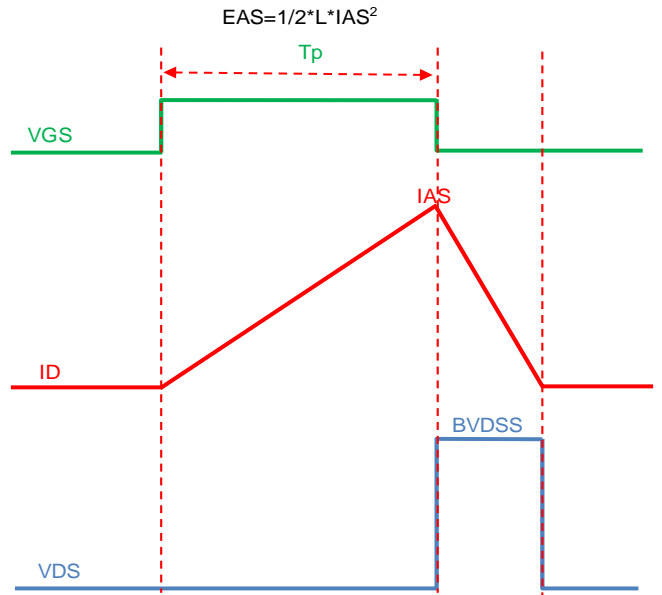


Figure A.



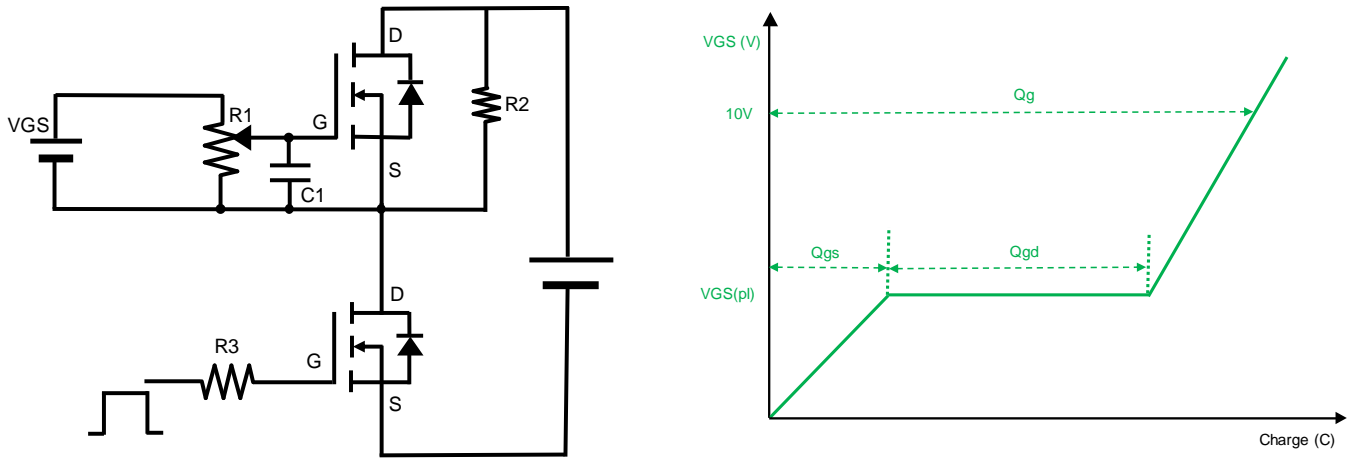


Figure B. Gate Charge Test Circuit & Waveform

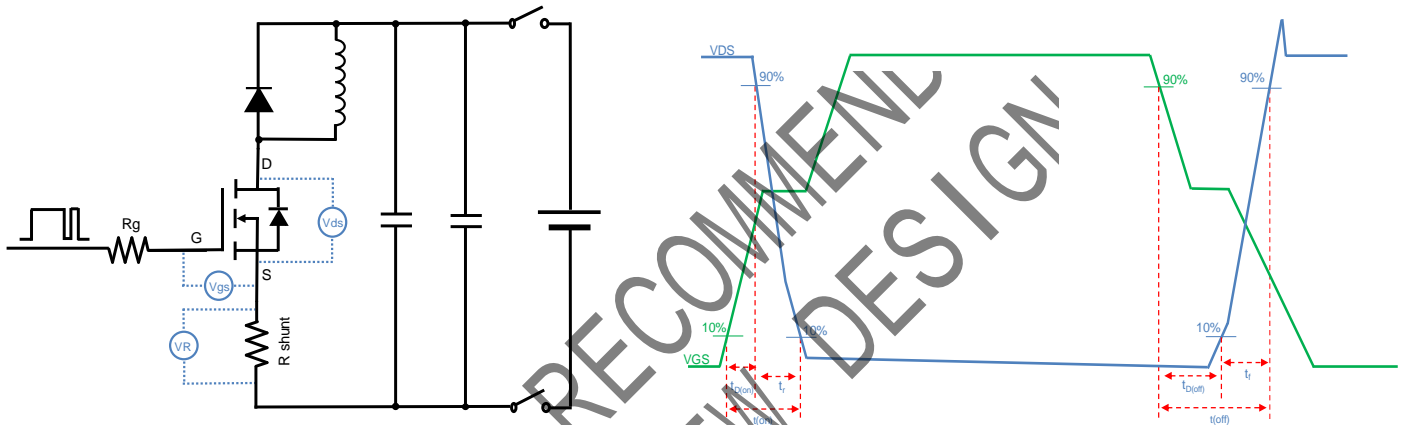


Figure C. Resistive Switching Test Circuit & Waveform

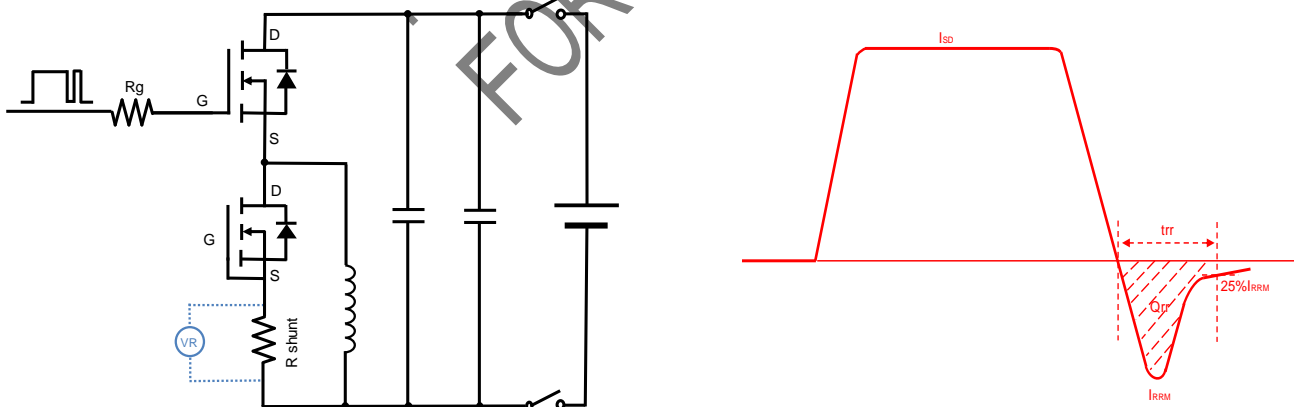
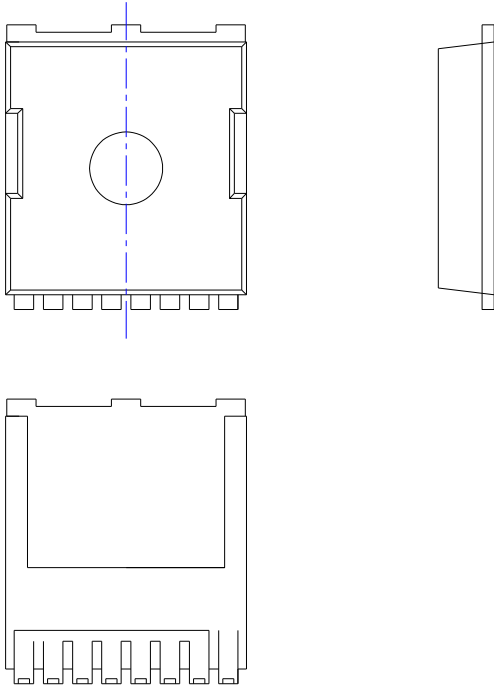


Figure D. Diode Recovery Test Circuit & Waveform



TOLL Package information
TYPE A



NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm

TYPE B:

NOT RECOMMEND
FOR NEW DESIGN

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	1.1	1.2	1.3
c	0.4	0.5	0.6
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.2	3.3	3.4
D3	4.45	4.55	4.65
E	9.8	9.9	10
E1	8	8.1	8.2
e	1.2 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
i	0.1 REF		
j	0.46 REF		
L	1.5	1.6	1.7
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.3	0.4	0.5
Q	8 REF		
R	3.0	3.1	3.2

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.03mm.
3.The pad layout is for reference purposes only.



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