N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	300A
$R_{DS(ON)}$(at V_{GS}=10V)	1.55m
$R_{DS(ON)}$(at V_{GS}=6V)	2.4m

100% EAS Tested

100% V_{DS} Tested

General Description

Excellent package for heat dissipation

High density cell design for low $R_{DS(ON)}$

Epoxy Meets UL 94 V-0 Flammability Rating

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D	2	2.6	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	1.2	1.55	
		V_{GS}=6V, I_D=15A	-	1.8	2.4	
Diode Forward Voltage	V_{SD}	I_S=30A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.35	-	
Maximum Body-Diode Continuous Current	I_S		-	-	300	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=100KHz	-	10411	-	pF
Output Capacitance	C_{oss}		-	1986	-	
Reverse Transfer Capacitance	C_{rss}		-	24.7	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=30A	-	166	-	nC
Gate-Source Charge	Q_{gs}		-	34	-	
Gate-Drain Charge	Q_{gd}		-	49	-	
Reverse Recovery Charge	Q_{rr}	I_F=30A, di/dt=100A/us	-	167	-	nC
Reverse Recovery Time	t_{rr}		-	92	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V, I_D=30A R_{GEN}=4.5	-	30	-	ns
Turn-on Rise Time	t_r		-	65	-	
Turn-off Delay Time	$t_{D(off)}$		-	121	-	
Turn-off fall Time	t_f		-	107	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25℃, V_{DD}=80V, V_G=10V, R_G 2mH, IAS=46A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of R is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.

Typical Electrical and Thermal Characteristics Diagrams

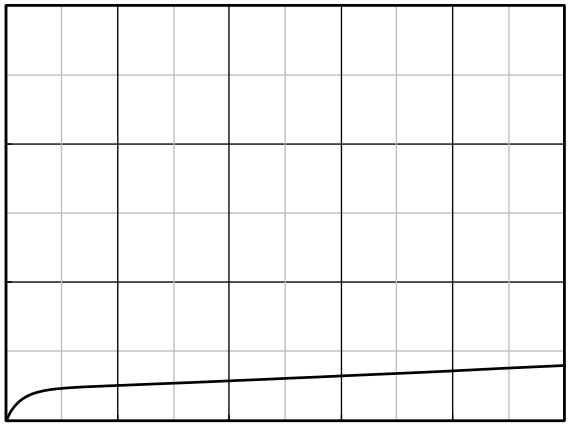

Figure 1. Output Characteristics

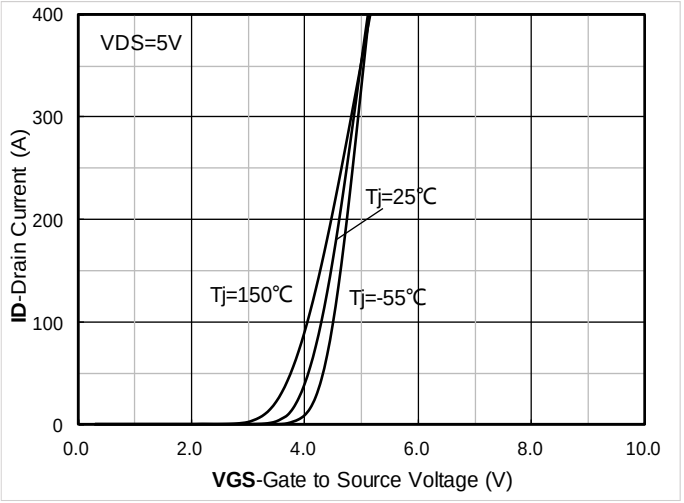

Figure 2. Transfer Characteristics

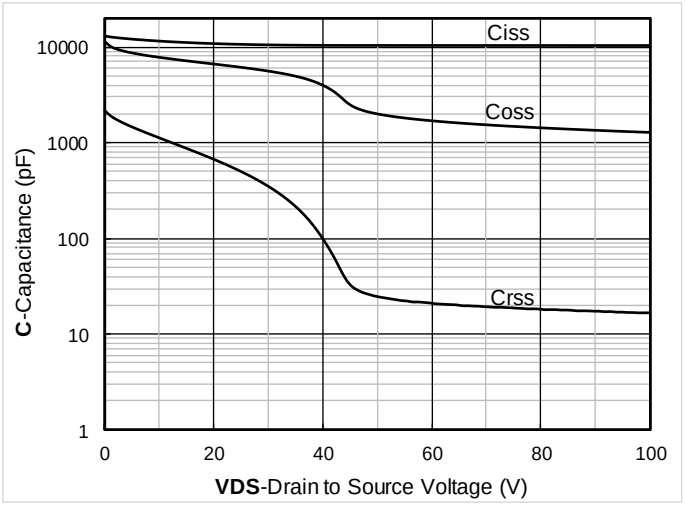

Figure 3. Capacitance Characteristics

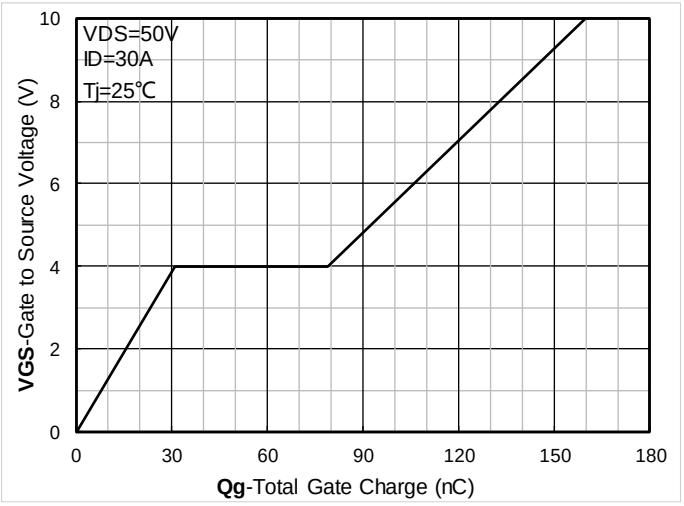

Figure 4. Gate Charge

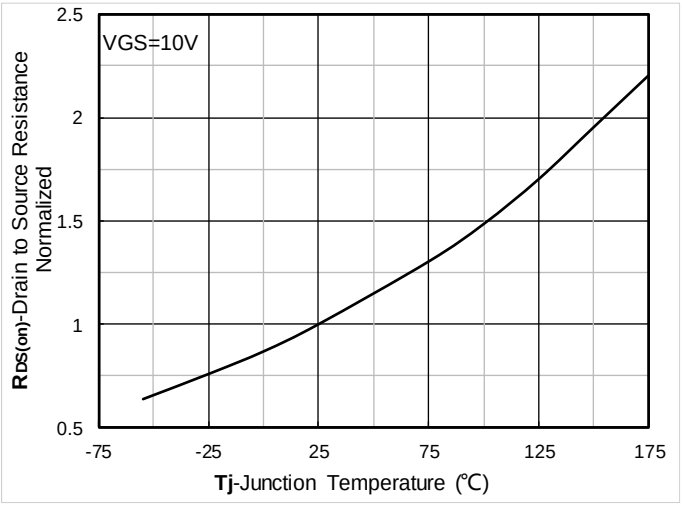

Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

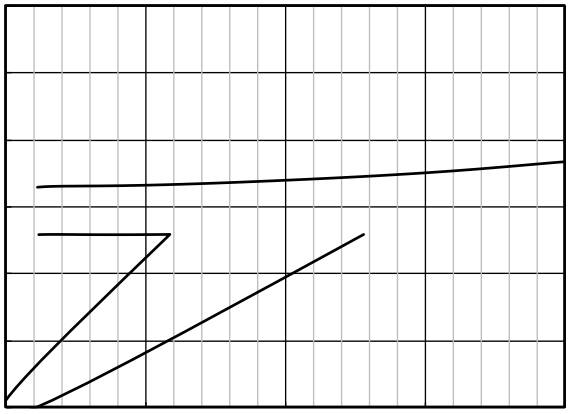

Figure 7. $R_{DS(on)}$ VS Drain Current

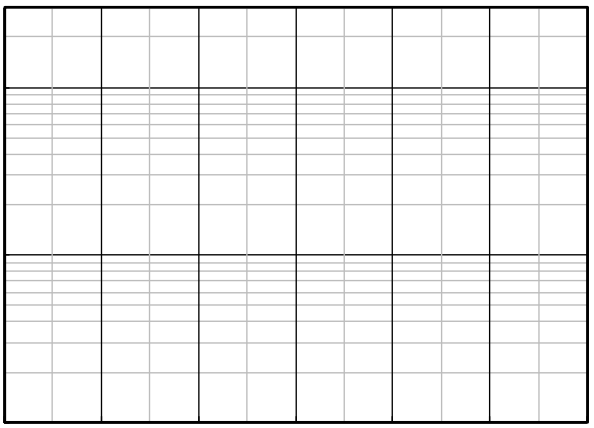

Figure 8. Forward characteristics of reverse diode

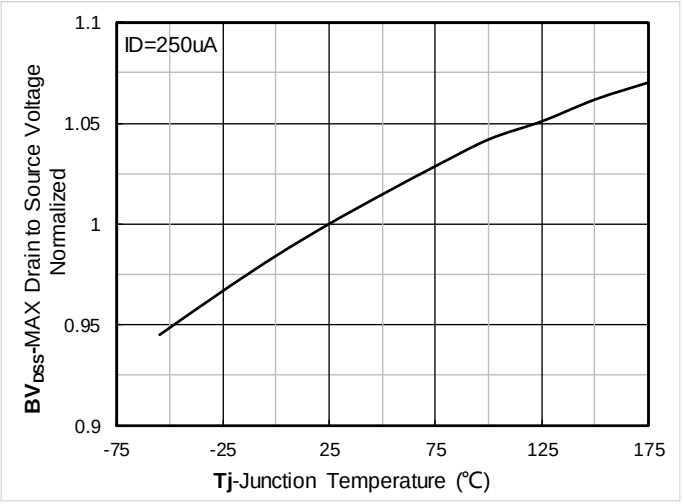

Figure 9. Normalized breakdown voltage

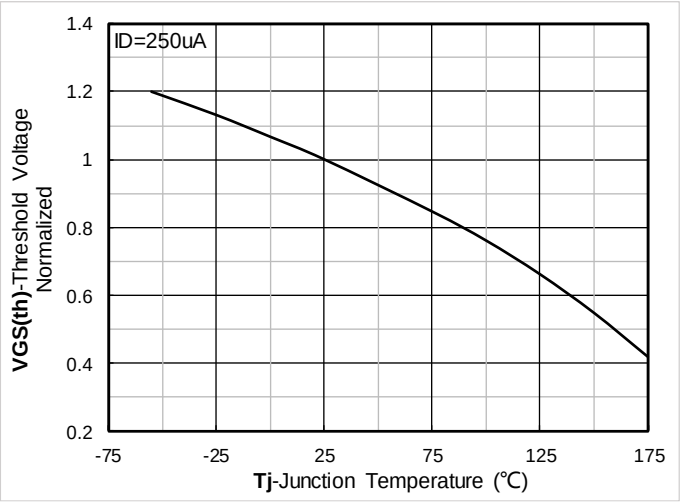

Figure 10. Normalized Threshold voltage

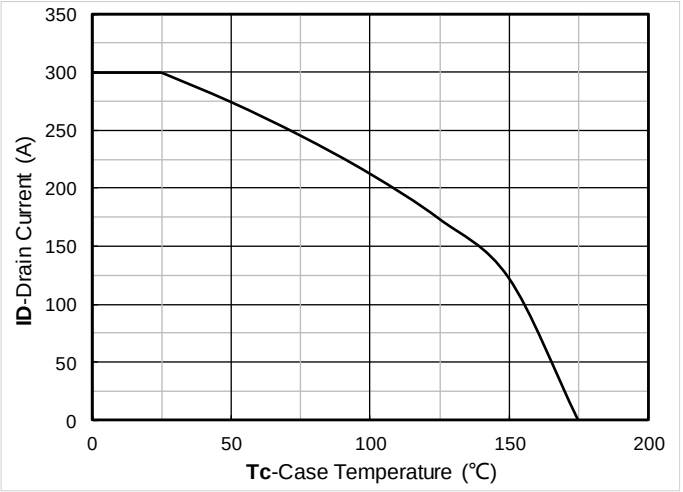

Figure 11. Current dissipation

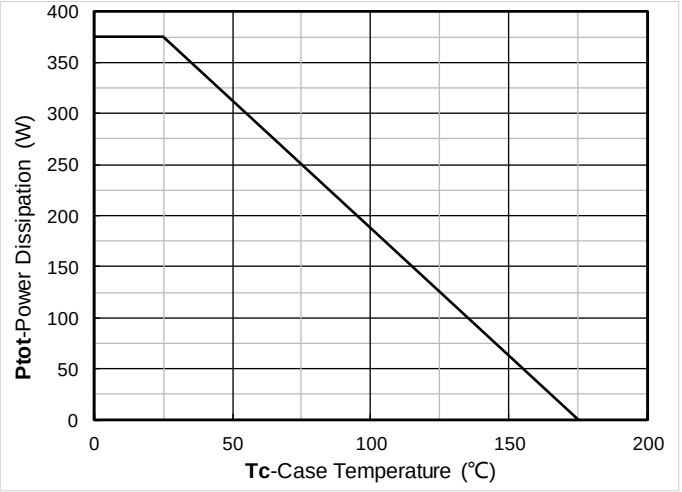

Figure 12. Power dissipation

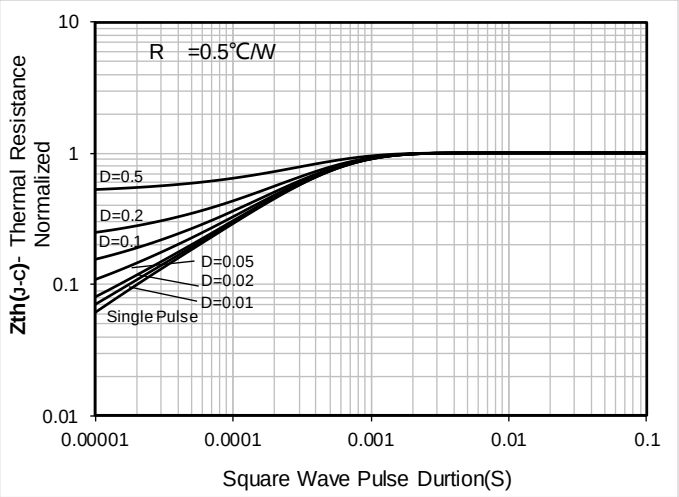

Figure 13. Maximum Transient Thermal Impedance

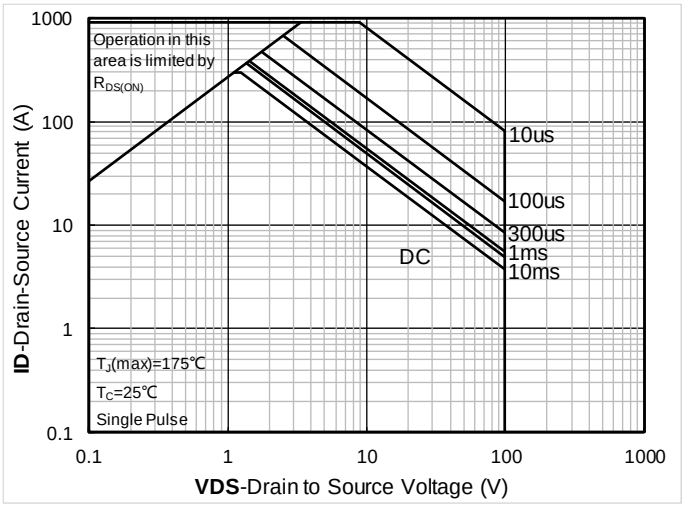

Figure 14. Safe Operation Area

Test Circuits & Waveforms

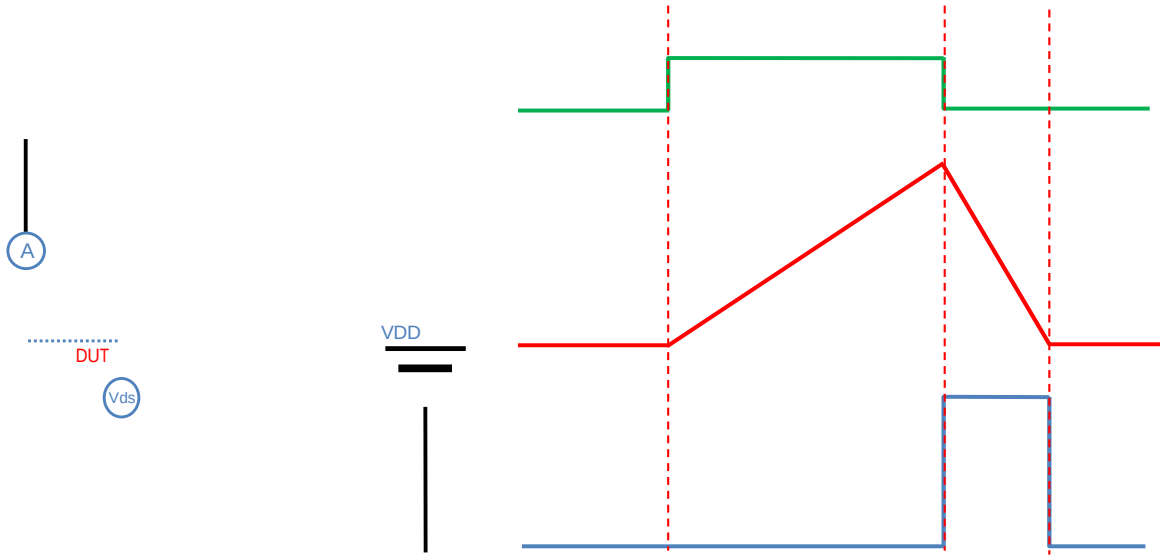

Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

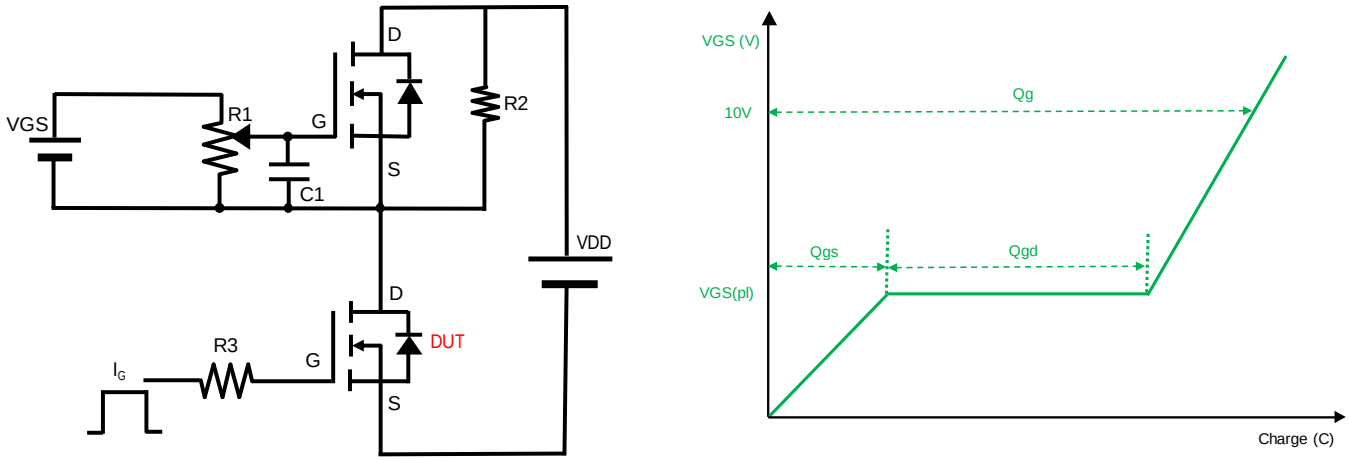

Figure B. Gate Charge Test Circuit & Waveform

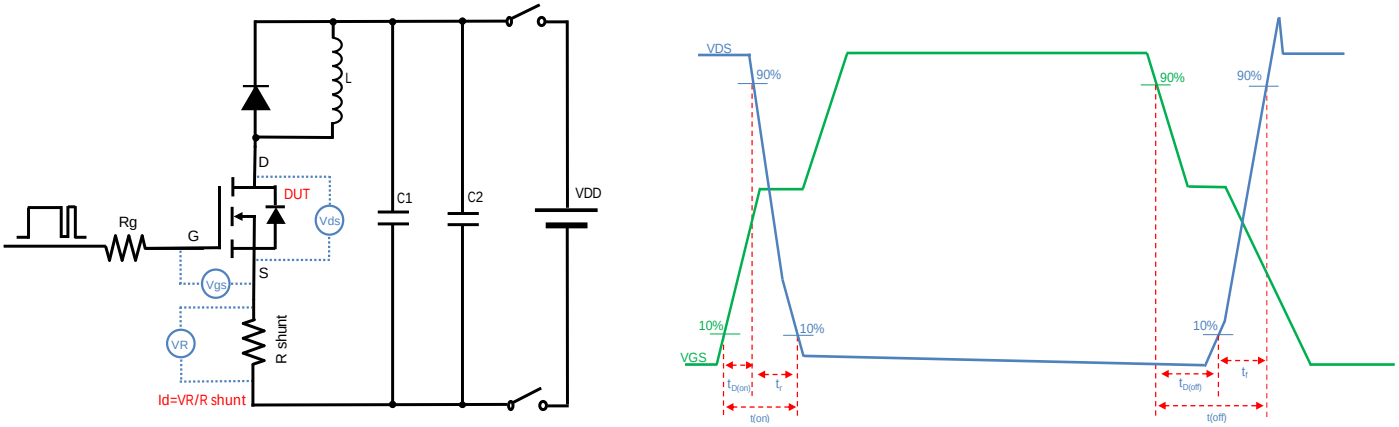

Figure C. Resistive Switching Test Circuit & Waveform

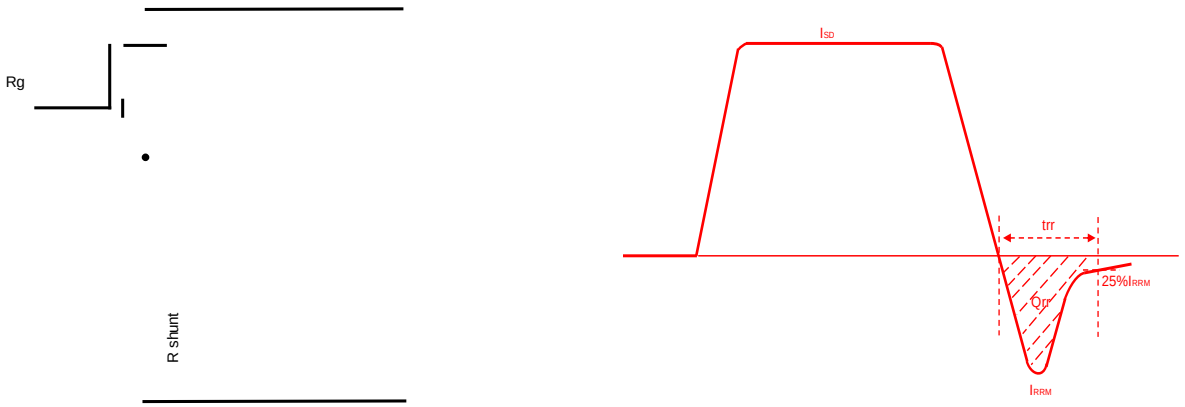

Figure D. Diode Recovery Test Circuit & Waveform

TOLL Package information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	1.1	1.2	1.3
c	0.4	0.5	0.6
D			

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.03mm.
3.The pad layout is for reference purposes only.

SUGGESTED SOLDER PAD LAYOUT
TOP VIEW

Disclaimer

The information prese